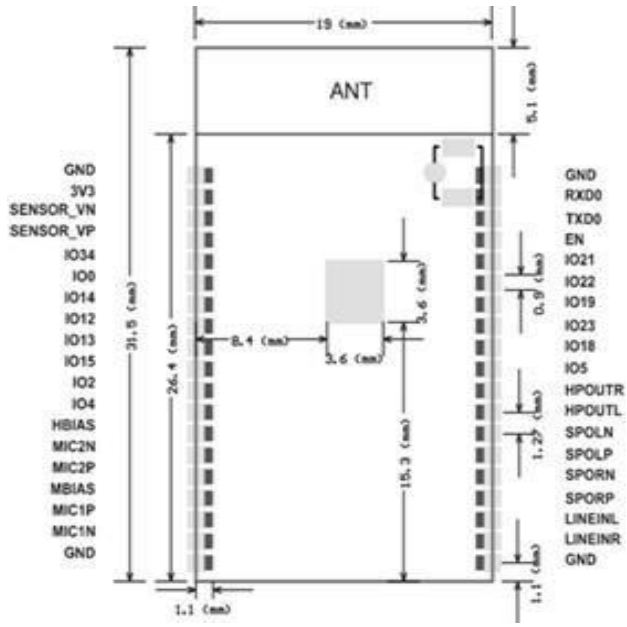
1.Product overview

ESP32-A1S is an ultra-small, powerful module.Built-in advanced low-power dual-core 32-bit CPU and CodeC audio decoding chip, it can be widely used in various IoT applications, suitable for home smart devices, smart audio, story machine solutions, etc. It is an ideal solution for IoT applications.

Internal circuit of ESP32-A1S module is highly integrated. It supports a variety of peripherals, secondary development and assists in achieving product differentiation features.

ESP32-A1S adopt SMD package. It can be used directly by plugging in the bottom plate, realizing rapid production of products and providing customers with high reliability.

Appearance size



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Characteristics

- Ultra-small 802.11b/g/n Wi-Fi + BT SoC module
- Using low-power dual-core 32-bit CPU, can be used as an application processor
- The main frequency is up to 240MHz, and the computing power is up to 600DMIPS
- Built-in 520KB SRAM, External 4MPSRAM
- Support UART/SPI/I2C/PWM/ADC/DAC
- Adopt SMD-38package, which is convenient for welding and testing
- Built-in CodeC audio decoder chip, can support music playback and recording
- Support multiple sleep modes, the minimum deep sleep current can reach 6.5uA
- Support STA/AP/STA+AP operating mode
- Support Smart Config/AirKiss one-click distribution network
- Common AT command can be used easy and quick
- Support serial port local upgrade and remote firmware upgrade (FOTA)
- Embedded Lwip and FreeRTOS
- Support a variety of mainstream compression and lossless audio formats, including M4A, AAC, FLAC, OGG, OPUS, MP3, etc.
- Support Wi-Fi, BT-audio, DLNA, Line-in and other audio source input

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Main parameters

Table 1 main parameters instruction

Model	ESP32-A1S(AC101 version）
Package	SMD-38
Size	32*19*3 mm
Certification	FCC/CE
SPI Flash	Default 32Mbit, maximum support 128Mbit
Audio format	M4A、AAC、FLAC、OGG、OPUS、MP3、WAV、RA、VQF etc,.
Audio output	Support 1 headphone output and 1 left and right speaker output
Audio input	Support 3 analog microphone inputs
IO	14
UART rate	Support 300 ~ 4608000 bps， default 115200bps
Bluetooth	Bluetooth 4.2 BR/EDR and stander BLE, support A2DP,AVRC etc,.
Wi-Fi	802.11 b/g/n/e/i, support DLNA
On-chip sensors	Hall sensor、Temperature sensor、Capacitive touch sensor
Spectrum range	2412 ~2484MHz
Antenna	On-board PCB antenna/ IPEX
Transmit power	802.11b: 17±2 dBm (@11Mbps) 802.11g: 14±2 dBm (@54Mbps) 802.11n: 13±2 dBm (@MCS7)
Receiving sensitivity	CCK, 1 Mbps : -90dBm CCK, 11 Mbps: -85dBm 6 Mbps (1/2 BPSK): -88dBm 54 Mbps (3/4 64-QAM): -70dBm MCS7 (65 Mbps, 72.2 Mbps): -67dBm
Power consumption (typical value)	350mA
Security	WPA/WPA2/WPA2-Enterprise/WPS
Power supply range	Voltage 3.0V ~ 3.6V, current >500mA
Operating temperature	-20 ℃ ~ 85℃
Storage environment	-40 ℃ ~ 85℃ , < 90%RH
Weight	2.5±0.05g

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2. Pin function

ESP32-A1S module is connected to 38 interfaces, table 2.1 and table 2.2 is the interface definition.

table 2.1 ESP32-A1S Pin diagram

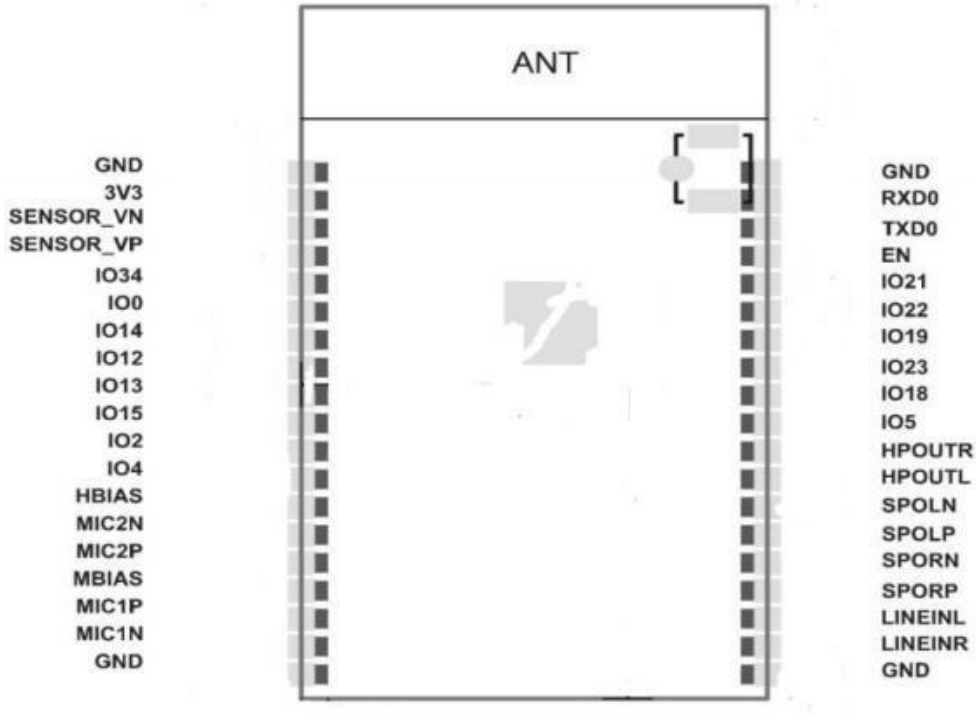


table 2.2 pin function definition

No.	Pin	Function Description
1	GND	Ground
2	3V3	3.3V power supply（VDD）; The output current of the external power supply is recommended to be above 500mA
3	SENSOR_VN	GPI39,SENSOR_VN,ADC1_CH3,ADC_H,RTC_GPIO3
4	SENSOR_VP	GPI36,SENSOR_VP,ADC_H,ADC1_CH0,RTC_GPIO0
5	IO34	GPI34,ADC1_CH6,RTC_GPIO4
6	IO0	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
7	IO14	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
8	IO12	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
9	IO13	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
10	IO15	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3
11	IO2	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SDS_DATA0

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12	IO4	GPIO4,ADC2_CH0,TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
13	HBIAS	MIC2 control pin
14	MIC2N	MIC2 input
15	MIC2P	MIC2 input
16	MBIAS	MIC1 control pin
17	MIC1P	MIC1 input
18	MIC1N	MIC1 input
19	GND	Ground
20	GND	Ground
21	LINEINR	Headphone input
22	LINEINL	Headphone input
23	SPORP	Speaker right channel output
24	SPORN	Speaker right channel output
25	SPOLP	Speaker left channel output
26	SPOLN	Speaker left channel output
27	HPOUTL	Headphone output
28	HPOUTR	Headphone output
29	IO5	GPIO5,VSPICS0,HS1_DATA6,EMAC_RX_CLK
30	IO18	GPIO18,VSPICLK,HS1_DATA7
31	IO23	GPIO23,VSPID,HS1_STROBE
32	IO19	GPIO19,VSPIQ,U0CTS,EMAC_TXD0
33	IO22	GPIO22,VSPIWP,U0RTS,EMAC_TXD1
34	IO21	GPIO21,VSPIHD,EMAC_TX_EN
35	EN	Enable chip, active high
36	TXD0	GPIO1,U0TXD,CLK_OUT3,EMAC_RXD2
37	RXD0	GPIO3,U0RXD,CLK_OUT2
38	GND	Ground

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Strapping Pin

Build-in LDO (VDD_SDIO) voltage			
Pin	Default	3.3V	1.8V
MTDI/GPIO12	Pull down	0	1
System startup method			
Pin	Default	SPI Flash startup method	Download start mode
GPIO0	Pull up	1	0
GPIO2	Pull down	/	0
Note: The working voltage of the built-in flash is 3.3V, and the MTDI needs to be pulled down or left floating when powering on the chip with built-in flash			

3. Function description

CPU and RAM

ESP32 contains two low-power Xtensa®32-bit LX6 MCUs. On-chip storage includes:

- 448KBytes ROM for program startup and kernel function call
- 520 KB on-chip SRAM for data and instruction storage
- 8KBytes of SRAM in RTC (RTC slow memory) can be accessed by the coprocessor in Deep-sleep mode
- The 8KBytes of SRAM in RTC, that is, RTC fast memory, can be used for data storage and accessed by the main CPU during RTC startup in Deep-sleep mode
- 1kbit EFUSE, of which 256 bits are dedicated to the system (MAC address and chip settings); the remaining 768 bits are reserved for user applications, which include Flash encryption and chip ID

External Flash and SRAM

ESP32 supports up to four 16 MBytes external QSPI Flash and static random access memory (SRAM), and has a hardware encryption function based on AES to protect developers' programs and data.

- ESP32 accesses external QSPI Flash and SRAM through cache. Up to 16 MBytes of external Flash is mapped to the CPU code space, supporting 8-bit, 16-bit and 32-bit access, and executable code
- Up to 8M Bytes of external Flash and SRAM are mapped to the CPU data space, supporting 8-bit, 16-bit and 32-bit access. Flash only supports read operations, SRAM can support read and write operations

Codec

AC101 is a highly integrated audio codec chip with high mixed signal integration. The integrated digital phase-locked loop supports a wide range of input/output frequencies. It can generate the audio clock required by the codec from the standard audio crystal rates of 22.5792MHz and 24.576MHz.

- 2 ADCs and 2 DACs @ 24 bits and interphase locked loop processing with flexible clocking scheme
- The signal-to-noise ratio during the playback path of the digital-to-analog converter can reach up to 100dB
- The signal-to-noise ratio is as high as 95dB during the recording path
- Capacitor-free stereo headphone driver, 18mW@1.8V
- Two stereo differential speaker outputs\
- Two low-noise analog microphone offsets

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- TWI/RSB control interface
- A 24-bit 8KHz~192KHz I2S/PCM interface
- Support digital copyright control of digital-to-analog converter playback output
- Soft mute circuit to suppress popping

Crystal oscillator

Supports crystal oscillators with frequencies of 40 MHz, 26 MHz and 24 MHz. The accuracy of the crystal oscillator is between ±10 PPM, and the operating temperature range is between -40° C and 85° C. Please select the correct crystal type when using the download tool. In the circuit design, the ground adjustment capacitors C1 and C2 are added to the input and output terminals of the crystal oscillator, respectively. The value of the two capacitors can be flexibly set, ranging from 6 pF to 22 pF. However, the specific capacitance value can only be determined after matching the overall performance of the entire circuit. Generally speaking, if the frequency of the crystal oscillator is 26 MHz, the capacitance values of C1 and C2 are within 10 pF; if the frequency of the crystal oscillator is 40 MHz, the capacitance values of C1 and C2 are 10 pF<C1, C2<22 pF. The frequency of the RTC crystal oscillator is usually 32 kHz or 32.768 kHz. Due to the internal calibration used to correct the frequency offset, the frequency of the crystal oscillator may exceed the range of ±20 PPM. When the chip is working in low-power mode, the device should select an external low-speed 32 kHz crystal oscillator clock instead of the internal RC oscillator to obtain an accurate wake-up time.

Power consumption

ESP32 has advanced power management technology that can switch between various power saving modes

- Active mode: The chip's radio frequency is in working condition. The chip can receive, transmit and listen to signals
- Modem-sleep mode： The CPU keeps running and the clock can be configured. Wi-Fi/Bluetooth baseband and radio frequency off
- Light-sleep mode： The CPU is suspended. RTC and ULP coprocessors run. Any wake-up event (MAC, host, RTC timer or external interrupt) will wake up the chip

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4. Electrical parameters

ESP32-A1S series modules are electrostatic sensitive devices, special precautions need to be taken when handling



Unless otherwise specified, the test environment for the specifications listed in this chapter is：VBAT= 3.3V,TA= 27℃

Limit parameters：

Rated value	Condition	Value	Unit
Storage temperature	-	-40~85	℃
Maximum welding temperature	-	260	℃
Supply voltage	IPC/JEDEC J-STD-020	+3.0~+3.6	V

Recommended working conditions：

Working environment	Name	Min	Typical value	Max	Unit
Operating temperature	-	-40	20	85	℃
Supply voltage	VDD	3.0	3.3	3.6	V

Digital port characteristics:

Port	Name	Min	Typical value	Max	Unit
Input logic level is low	VIL	-0.3	-	0.25VDD	V
Input logic level is high		0.75VDD	-	VDD+0.3	V
Out put logic level is low	VOL	N	-	0.1VDD	V
Output logic level is high		0.8VDD	-	N	V

Wi-Fi RF characteristics:

Description	Min	Typical value	Max	Unit
General features				
Input frequency	2412	-	2484	MHz
Input resistance	-	50	-	Ω
Input launch	-	-	-10	dB
PA output power	15.5	16.5	21.5	dBm
Sensitivity				
DSSS,1Mbps	-	-98	-	dBm
CCK, 11 Mbps	-	-90	-	dBm
OFDM, 6 Mbps	-	-93	-	dBm
OFDM, 54 Mbps	-	-75	-	dBm
HT20, MCSO	-	-93	-	dBm
HT20, MCS7	-	-73	-	dBm
HT40, MCSO	-	-90	-	dBm
HT40, MCS7	-	-70	-	dBm

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MCS32	-	-91	-	dBm
Adjacent Channel Suppression				
OFDM, 6 Mbps	-	37	-	dB
OFDM, 54 Mbps	-	21	-	dB
HT20, MCS0	-	37	-	dB
HT20, MCS7	-	20	-	dB

BLE receiver features:

Parameter	Condition	Min	Typical value	Max	Unit
Sensitivity@ 0.1% BER	-	-	-98	-	dBm
Max received signal@0.1% BER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-5	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
Out-of-band blocking performance	30MHz-2000MHz	-10	-	-	dBm
	2000MHz-2400MHz	-27	-	-	dBm
	2500MHz-3000MHz	-27	-	-	dBm
	3000MHz-12.5GHz	-10	-	-	dBm
Intermodulation performance	-	-36	-	-	dBm

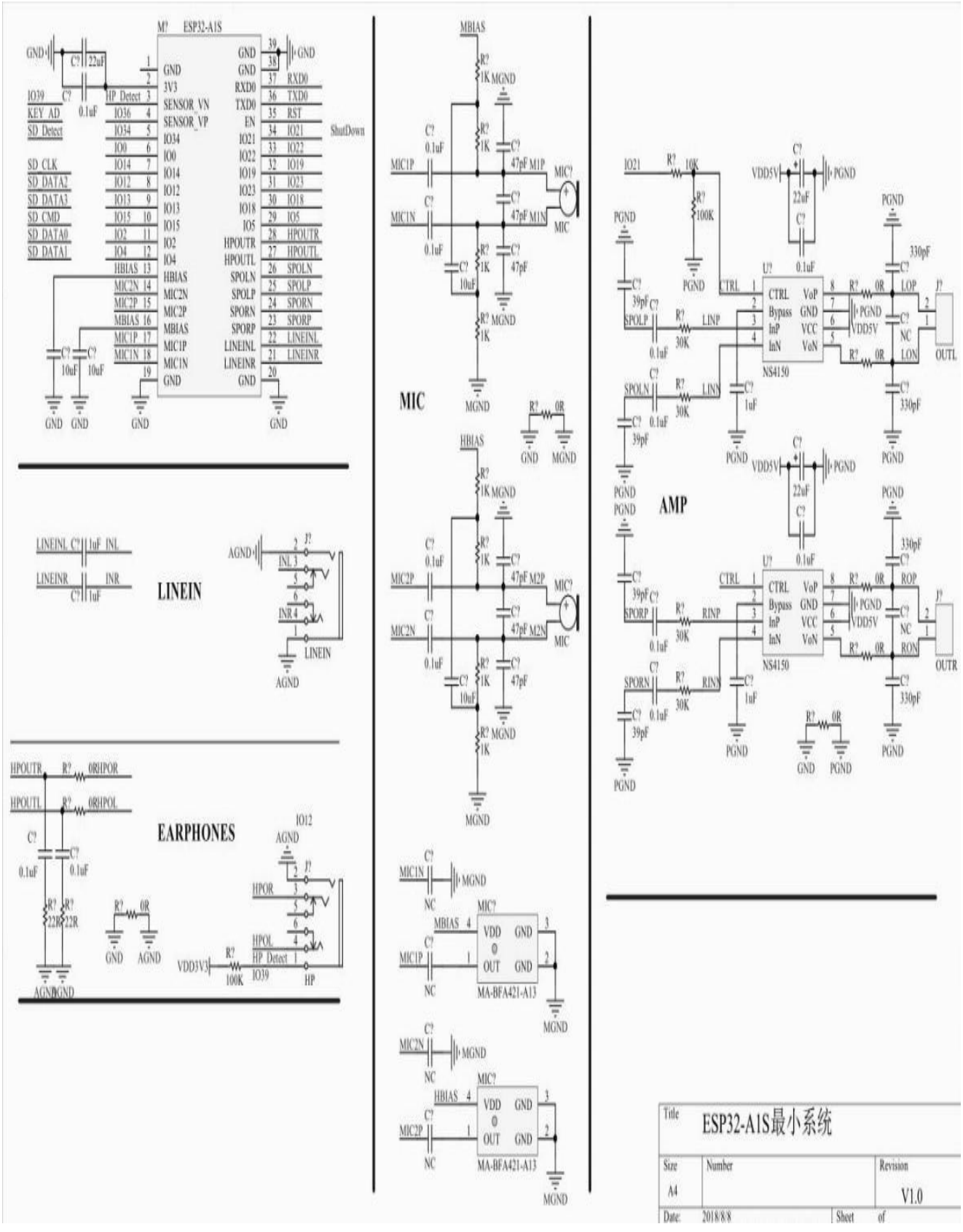
BLE transmitter characteristics:

Parameter	Condition	Min	Typical value	Max	Unit
RF transmit frequency	-	-	+7.5	+10	dBm
RF power control range	-	-	25	-	dB
Adjacent channel transmit power	F = F0 + 1 MHz	-	-14.6	-	dBm
	F = F0 - 1 MHz	-	-12.7	-	dBm
	F = F0 + 2 MHz	-	-44.3	-	dBm
	F = F0 - 2 MHz	-	-38.7	-	dBm
	F = F0 + 3 MHz	-	-49.2	-	dBm
	F = F0 - 3 MHz	-	-44.7	-	dBm
	F = F0 + > 3 MHz	-	-50	-	dBm
	F = F0 - > 3 MHz	-	-50	-	dBm
Δf1avg	-	-	-	265	kHz
Δf2max	-	247	-	-	kHz
Δf2avg/Δf1avg	-	-	-0.92	-	-
ICFT	-	-	-10	-	kHz
Frequency drift rate	-	-	0.7	-	kHz/50us
Frequency drift	-	-	2	-	kHz

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5. Design guidance

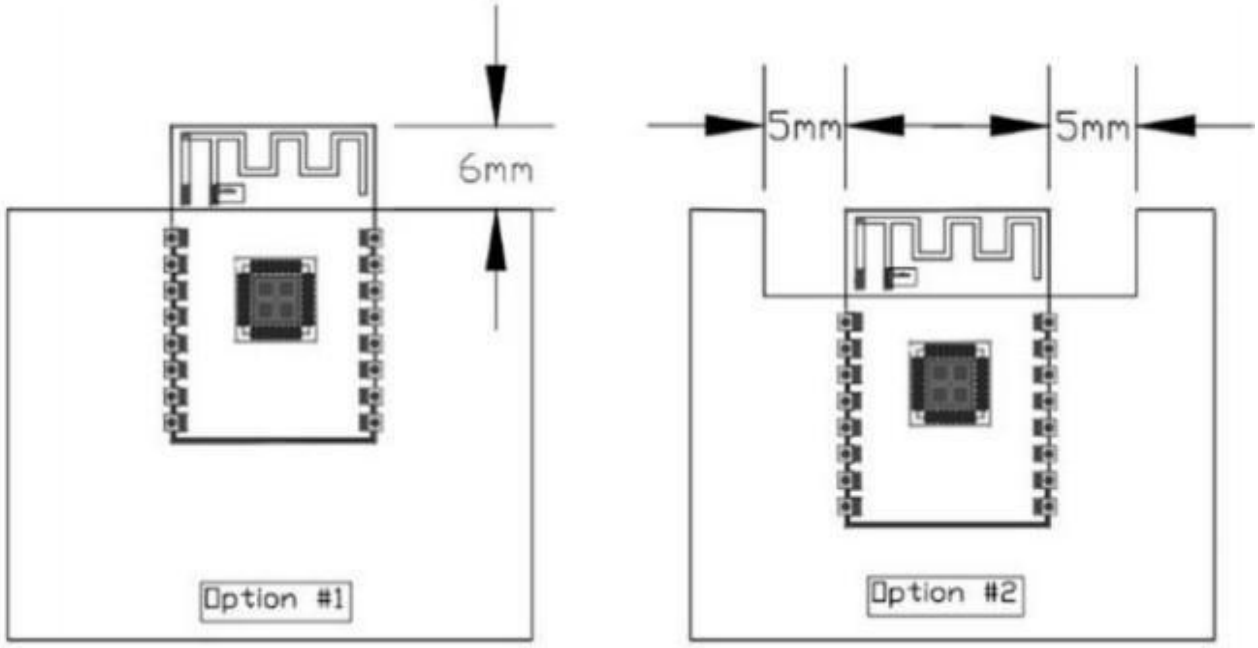
5.1 Application circuit



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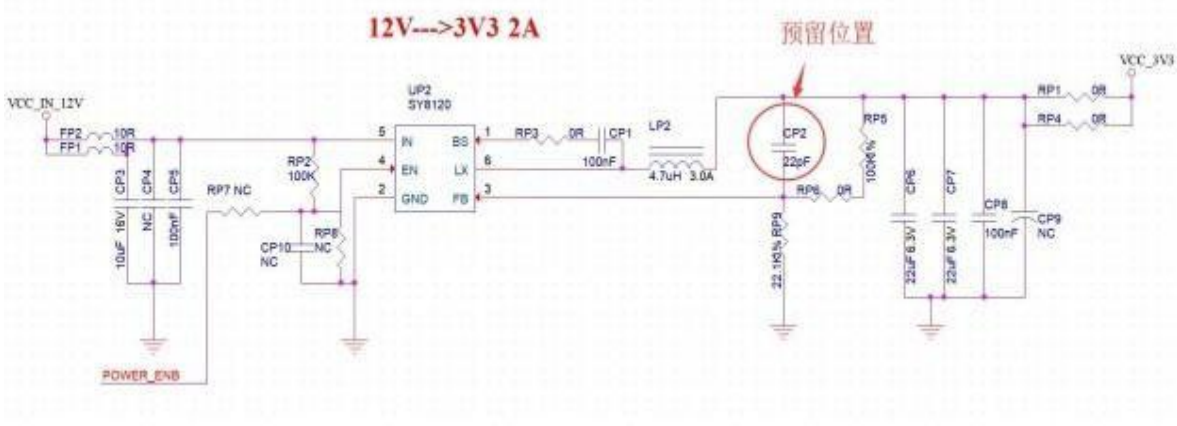
5.2 Antenna layout requirements

(1) For the installation position on the motherboard, the following two methods are recommended:
Solution 1: Put the module on the edge of the main board, and the antenna area extends out of the edge of the main board.
Solution 2: Put the module on the edge of the motherboard, and hollow out an area at the antenna position on the edge of the motherboard.
(2)In order to meet the performance of the on-board antenna, it is forbidden to place metal parts around the antenna.



5.3 Power supply

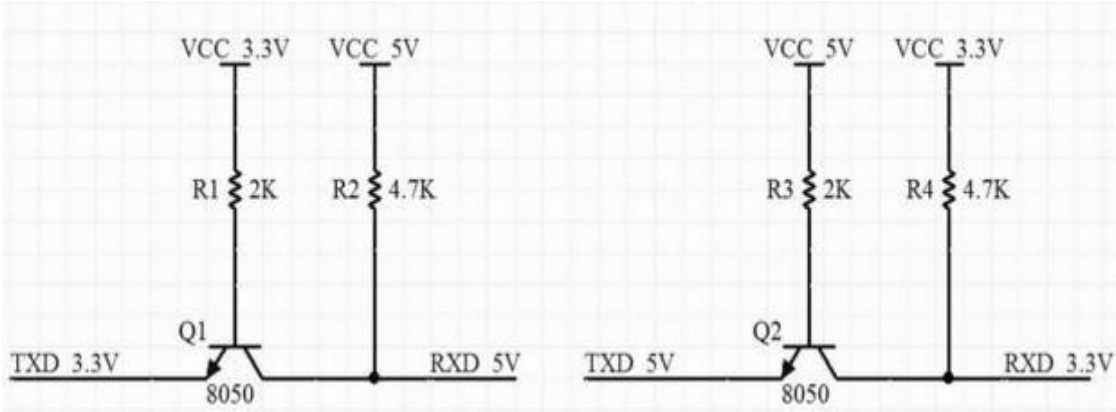
(1) Recommended 3.3V voltage, peak current above 500mA
(2) It is recommended to use LDO for power supply; if using DC-DC, it is recommended that the ripple be controlled within 30mV.
(3) The DC-DC power supply circuit is recommended to reserve the position of the dynamic response capacitor, which can optimize the output ripple when the load changes greatly.
(4) It is recommended to add ESD devices to the 3.3V power interface.



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5.4 Use of GPIO port

(1) There are some GPIO ports on the periphery of the module. If you need to use it, it is recommended to connect a 10-100 ohm resistor in series with the IO port. This can suppress overshoot and make the levels on both sides more stable. It is helpful for EMI and ESD.
(2) For the pull-up and pull-down of special IO ports, please refer to the instructions in the specification. This will affect the startup configuration of the module.
(3)The IO port of the module is 3.3V. If the main control and the IO level of the module do not match, you need to add a level conversion circuit.
(4)If the IO port is directly connected to a peripheral interface, or a terminal such as a header, it is recommended to reserve an ESD device near the terminal of the IO trace.

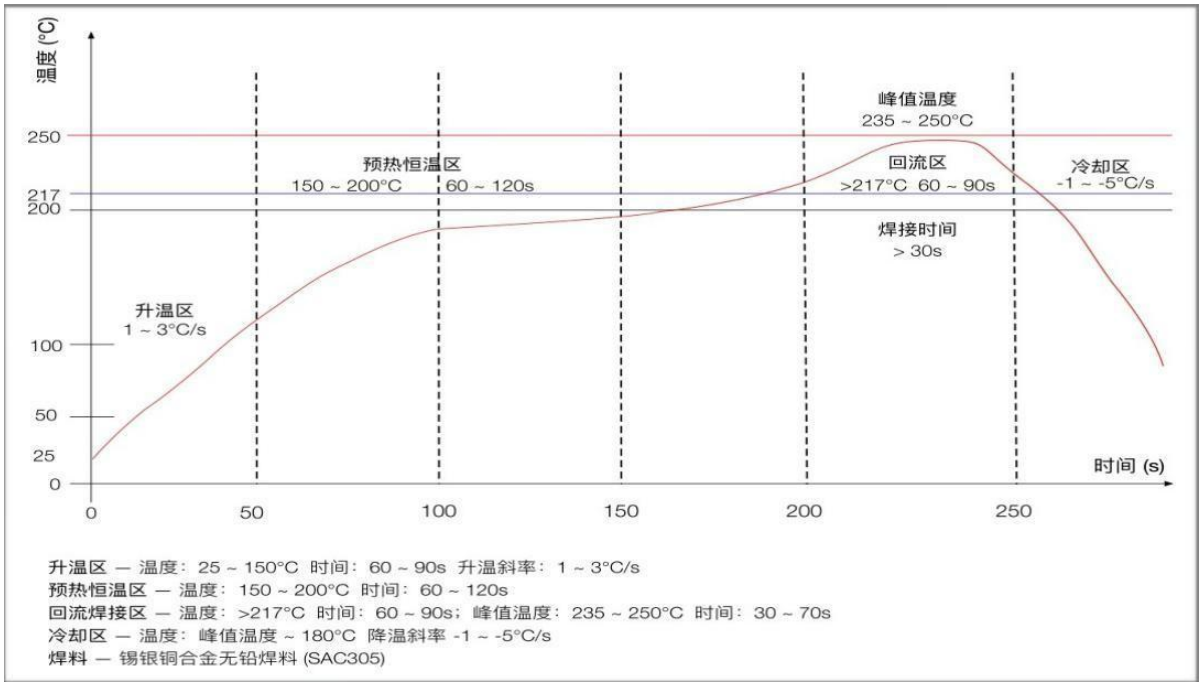


6. Module internal chip connection table

Chip / Interface	ESP32	AC101
I2S Pin connection	IO35	I2S_SOUT
	IO25	I2S_SDIN
	IO26	I2S_LRCK
	IO27	I2S_BCLK
	IO0	I2S_MCLK
I2C Pin connection	IO32	SCL
	IO33	SDA

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7. Reflow soldering curve



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8. Package Information

As shown in the figure below, the packaging of ESP32-A1S is tape.



9. Contact us

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Development DOCS：https://docs.ai-thinker.com

Official Forum：http://bbs.ai-thinker.com

Sample purchase：https://ai-thinker.en.alibaba.com/

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